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10/826,991	04/19/2004	John C. Wang	3304.2.127	3497

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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,991	WANG ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined and rejected.

Specification

2. The disclosure is objected to because of the following informalities. Appropriate correction is required.

2-1. To be consistent with Fig. 2, it appears that the "input keyboard 21", as shown in lines 2 and 6 of paragraph [0033], should be "keyboard 23". Also, the "display 23", as shown in lines 2 and 7 of paragraph [0033], should be "display 21".

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2, 5-7, 13-16, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4-1. Claim 2 recites the limitations "accumulating execution time of said simulating elements" in line 2 of the claim and "said execution time" in line 4 of the claim. It is indefinite because it is unclear whether "said execution time" is referred to (1) the execution time of each individual simulating element or (2) the accumulated execution time of all the simulating elements.

4-2. Claims 5-7 recite the limitation "the simulated hardware" in line 4 of each claim. There is insufficient antecedent basis for this limitation in the claim.

4-3. Claim 13 recites the limitation "the operations of said simulating elements" in lines 3-4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

4-4. Claim 14 recites the limitation "the simulated hardware" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

4-5. Claims 15-16 recite the limitation "said expected time point" in lines 1-2 of each claim. There is insufficient antecedent basis for this limitation in the claim.

4-6. Claims 15-16 recite the limitation "the simulated hardware" in lines 3-4 of each claim. There is insufficient antecedent basis for this limitation in the claim.

4-7. Claim 19 recites the limitation "the operations of said simulating elements" in lines 3-4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5, 8-10, and 12-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Elias, U.S. Patent 6,980,945 B2 issued December 27, 2005, and filed December 4, 2001.

6-1. Regarding claim 1, Elias discloses a timing control method of a hardware-simulating program, a plurality of simulating elements being defined in said hardware-simulating program and executed in a predetermined sequence, said timing control method comprising steps of:

referring to a time coordinate to realize a current time point when said hardware-simulating program has been executed to a certain degree (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45); and

suspending and then restarting operations of said simulating elements if said current time point has not reached a specified time point yet (the next-flag signal is scheduled to be turned on at time $t=t_{i-1}$+elapsed_time, column 4, lines 33-45).

6-2. Regarding claim 2, Elias further discloses comprising steps of:

accumulating execution time of said simulating elements (an updated elapsed time value for completing the instruction is determined and accumulated, column 4, lines 15-22); and

determining said hardware-simulating program has been executed to said certain degree when said execution time has reached or exceeded a threshold period (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45).

6-3. Regarding claim 3, Elias further discloses wherein said simulating elements are executed piecewise in said predetermined sequence (represent the sequential operations of the software program for controlling the modeled hardware, column 3, lines 54- 61), respective execution time of said simulating elements is accumulatively counted (an updated elapsed time value for completing the instruction is determined and accumulated, column 4, lines 15-22), and said certain degree is determined when accumulated execution time of each of said simulating

elements has reached or exceeded said threshold period (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45).

6-4. Regarding claim 4, Elias further discloses wherein a period from the simulation starting point to said specified time point is a multiple or reciprocal multiple of said threshold period (Both software timeline 20 and hardware timeline 30 start at the same time point t_0 and operate in parallel, column 3, lines 35-36).

6-5. Regarding claim 5, Elias further discloses wherein said period from the simulation starting point to said specified time point is equal to said threshold period so that the simulation speed of said hardware-simulating program is equal to that of the simulated hardware (Both software timeline 20 and hardware timeline 30 start at the same time point t_0 and operate in parallel, column 3, lines 35-36).

6-6. Regarding claim 8, Elias further discloses wherein said hardware-simulating program is for simulating an instruction set executed when a microcontroller controls a plurality of peripheral devices (modeling of the MCU and of the device it controls, column 3, lines 7-11), and said execution time of said simulating elements is accumulated by operating the count of executed machine commands with a machine cycle of said microcontroller (the time value for completing each instruction in the operating program is calculated based on data published in the documentation for the MCU through which the operating program is implemented, column 4, lines 22-26).

6-7. Regarding claim 9, Elias further discloses wherein said operations of said simulating elements are restarted when said specified time point has been reached (the next-flag signal is scheduled to be turned on at time $t=t_{i-1}$+elapsed_time, column 4, lines 33-45).

6-8. Regarding claim 10, Elias further discloses wherein said time coordinate is a system clock (the system clock begins, column 3, lines 62-65).

6-9. Regarding claim 12, Elias discloses a timing control method of a hardware-simulating program, a plurality of simulating elements being defined in said hardware-simulating program and executed in a predetermined sequence, said timing control method comprising steps of:

referring to a time coordinate to realize a current time point when accumulated execution time of each of said simulating elements is equal to or greater than a threshold (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45); and

performing a time-compensating operation if said current time point does not conform to an expected time point (the next_flag is set to off, so that no further instructions are run, column 4, lines 33-45).

6-10. Regarding claim 13, Elias further discloses wherein when said current time point lags behind said expected time point, said time-compensating operation is performed by suspending the operations of said simulating elements (the next_flag is set to off, so that no further instructions are run, column 4, lines 33-45) until said current time point advances to conform to said expected time point (the next-flag signal is scheduled to be turned on at time $t=t_{i-1}$ + elapsed_time, column 4, lines 33-45).

6-11. Regarding claim 14, Elias further discloses wherein said expected time point is equal to said threshold so that the simulation speed of said hardware-simulating program is equal to that of the simulated hardware (Both software timeline 20 and hardware timeline 30 start at the same time point t_0 and operate in parallel, column 3, lines 35-36).

6-12. Regarding claim 15, Elias further discloses wherein said expected time point is a multiple of said threshold so that the simulated speed by said hardware-simulating program is a reciprocal multiple of that of the simulated hardware (Both software timeline 20 and hardware timeline 30 start at the same time point t_0 and operate in parallel, column 3, lines 35-36).

6-13. Regarding claim 16, Elias further discloses wherein said expected time point is a reciprocal multiple of said threshold period so that the simulated speed by said hardware-simulating program is a multiple of that of the simulated hardware (Both software timeline 20 and hardware timeline 30 start at the same time point t_0 and operate in parallel, column 3, lines 35-36).

6-14. Regarding claim 17, Elias discloses a recording medium recorded therein an accessible and executable hardware- simulating program, said hardware-simulating program defining therein a plurality of simulating elements, and said simulating elements being executed in a predetermined sequence and automatically synchronized at intervals with a time coordinate of a system executing said hardware-

simulating program, wherein said simulating elements are automatically synchronized by:

referring to said time coordinate to realize a current time point whenever said hardware-simulating program has been executed to a certain degree (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45); and

performing a time-compensating operation if said current time point does not conform to an expected time point (the next_flag is set to off, so that no further instructions are run, column 4, lines 33-45).

6-15. Regarding claim 18, Elias discloses a software platform for facilitating control program development, allowing a hardware-simulating program to work thereon, said hardware-simulating program defining therein a plurality of simulating elements, and said simulating elements being executed in a predetermined sequence and automatically synchronized at intervals with a time coordinate of a system executing said hardware-simulating program, wherein said simulating elements are automatically synchronized by:

referring to said time coordinate to realize a current time point whenever said hardware-simulating program has been executed to a certain degree (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45); and

performing a time-compensating operation if said current time point does not conform to an expected time point (the next_flag is set to off, so that no further instructions are run, column 4, lines 33-45).

6-16. Regarding claim 19, Elias further discloses wherein said time coordinate is referred to realize a current time point when accumulated execution time of each of said simulating elements is equal to or greater than a threshold (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45), the operations of said simulating elements are suspended when said current time point lags behind said expected time point (the next_flag is set to off, so that no further instructions are run, column 4, lines 33-45), and the operations of said simulating elements are restarted when said current time point advances to conform to said expected time point (the next-flag signal is scheduled to be turned on at time $t=t_{i-1}$+elapsed_time, column 4, lines 33-45).

6-17. Regarding claim 20, Elias further discloses wherein said accumulated execution time of each of said simulating elements is calculated by timing the count of executed machine commands with a machine cycle of the simulated hardware (the time value for completing each instruction in the operating program is calculated based on data published in the documentation for the MCU through which the operating program is implemented, column 4, lines 22-26).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6, 7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elias, U.S. Patent 6,980,945 B2 issued December 27, 2005, and filed December 4, 2001, in view of Hellestrand et al., U.S. Patent 6,230,114 B1 issued May 8, 2001.

8-1. Regarding claims 6 and 7, Elias discloses a timing control method in claim 4. Specifically, Elias discloses at column 3, lines 35-36, "Both software timeline 20 and hardware timeline 30 start at the same time point t_0 and operate in parallel." In other words, both timeline have the same time scale.

Elias fails to expressly disclose said period from the simulation starting point to said specified time point is double (a half) of said threshold period so that the simulated speed by said hardware-simulating program is a half (double) of that of the simulated hardware.

Hellestrand et al. disclose a hardware and software co-simulation design system including hardware simulator and processor simulators as shown in FIG. 2. Since simulation speed is extremely important, and since a single host processor can only process a single task at a time, Hellestrand et al. provide for carrying out the simulation in a host computer system that includes several host processors interconnected using a network connection and use the interface mechanism to handle the communication among simulators and processors (column 11, line 21-58). Furthermore, in this distributed simulation environment, "when several processor simulators operate, each processor simulator has its own concept of time, as does the hardware simulator." (column 8, lines 48-57). In other words, the simulation speed is independently adjustable.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Elias to incorporate the teachings of Hellestrand et al. to obtain the invention as specified in claims 6 and 7 because a multiprocessor host computer system would improve the simulation speed limited by a single host processor.

8-2. Regarding claim 11, Hellestrand et al. further disclose comprising steps of:

attaching time tags to simulation data associated with a specified simulating element (time delay information, column 10, lines 3-7);

storing said simulation data into a queue (to place events on an event queue, column 10, lines 7-9); and

reading out said simulation data from said queue according to said time tags when it is the turn of said specified simulating element to operate (until an event is reached, column 10, lines 9-16).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Reference to Shahabuddin et al., U.S. Patent Application Publication No. 2004/0102946 A1 published May 27, 2004, and filed August 6, 2003, is cited as disclosing a virtual real time (VRT) system.

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
September 24, 2006 H.D.

KAMINI SHAH
SUPERVISORY PATENT EXAMINER